- Processor 1 loads x into its register 5
- Processor 1 increments its register 5
- Processor 2 loads x into its register 5
- Processor 1 stores its register 5 into x
- Processor 2 increments its register 5
- Processor 2 stores its register 5 into x

Figure 18.8 A sequence of steps that can occur when two independent processors or cores access variable x in shared memory.